IN THE CLAIMS

Claims 1-19 (cancelled)

Claim 20 (previously presented): A CMOS comparator circuit comprising:

(a) a differential input stage including

i. a first input transistor having a gate coupled to receive a first input voltage signal, a source coupled to a tail current source, and a drain coupled to a junction between a source of a first cascode transistor and a drain of a first load transistor,

ii. a second input transistor having a gate coupled to receive the a second input voltage signal, a source coupled to the tail current source, and a drain coupled to a junction between a source of a second cascode transistor and a drain of a second load transistor,

iii. a bias source coupled to gates of the first and second cascode transistors, and circuitry for biasing gates of the first and second load transistors;

(b) a CMOS output stage including

i. a P-channel pull-up transistor and an N-channel pull-down transistor,

ii. a P-channel first transistor having a source coupled to a first supply voltage and a gate coupled to a first input terminal for receiving a first input current, and an N-channel second transistor having a source coupled to a second supply voltage and a gate coupled to a second input terminal for receiving a second input current,

iii. a P-channel third transistor having a source coupled to the first supply voltage, a gate coupled to the first input terminal, and a drain coupled to a gate of the pull-up transistor, and an N-channel fourth transistor having a source coupled to the second supply voltage and a gate coupled to the second input terminal,

iv. a first feedback circuit having an input coupled to the gate of the pull-up transistor and an output coupled to a gate of a P-channel fifth transistor having a source coupled to a drain of the first transistor and a drain coupled to a gate of the pull-down transistor and a drain of the second transistor, and a second feedback circuit having an input coupled to the gate of the pull-down transistor and an output coupled to a gate of an N-channel sixth transistor having a source coupled to a drain of the fourth transistor and a drain coupled to the gate of the pull-up transistor,

v. the first feedback circuit producing a first delayed signal on the gate of the fifth transistor which causes the fifth transistor to turn on the pull-down transistor a first predetermined amount of time after the pull-up transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor, the second feedback circuit producing a second delayed signal on the gate of the sixth transistor which causes the sixth transistor to turn on the pull-up transistor a second predetermined amount of time after the pull-down transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor; and

(c) an element for coupling a drain of the second cascode transistor to the first and second input terminals to supply the first and second input currents such that they represent the difference between the first and second input voltage signals.

Claims 21 (original): The CMOS comparator circuit of claim 20 including a class AB control circuit coupled between the first and second input terminals.

Claims 22 (currently amended): A CMOS comparator circuit comprising:

(a) a differential input stage including

i. a first input transistor having a gate coupled to receive a first input voltage signal, a source coupled to a tail current source and a drain coupled to a drain of a first load transistor,

ii. a second input transistor having a gate coupled to receive the a second input voltage signal, a source coupled to the tail current source and a drain coupled to a drain of a second load transistor,

iii. a bias source coupled to gates of the first and second cascode transistors, and circuitry for biasing gates of the first and second load transistors;

(b) a CMOS output stage including

i. a P-channel pull-up transistor and an N-channel pull-down transistor,

ii. a first feedback circuit having ~~a first~~ an input coupled to the drain of one of the first and second input transistors ~~and a second input coupled to a gate of the pull-up transistor~~, and an output coupled to a gate of the pull-down transistor,

iii. a second feedback circuit having ~~a first~~ an input coupled to the drain of one of the first and second input transistors ~~and a second input coupled to the gate of the pull-down transistor~~, and an output coupled to the gate of the pull-up transistor,

iv. the first feedback circuit producing a first delayed signal on the gate of the pull-down transistor to turn on the pull-down transistor a first predetermined amount of time after the pull-up transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor, and

v. the second feedback circuit producing a second delayed signal on the gate of the pull-up transistor to turn on the pull-up transistor a second predetermined

amount of time after the pull-down transistor is turned completely off so as to prevent any shoot-through current from flowing through the pull-up transistor and the pull-down transistor.

Claim 23 (currently amended): The CMOS output stage of claim 22 wherein the ~~first~~ input of the first feedback circuit is coupled to the drain of one of the first and second input transistors by means of a first cascode transistor.

Claim 24 (currently amended): The CMOS output stage of claim 23 wherein the ~~first~~ input of the second feedback circuit is coupled to the drain of the other of the ~~first and second~~ input transistors by means of a second cascode transistor.